ENGLISH TRANSLATION OF INTERNATIONAL APPLICATION AS ORIGINALLY FILED

DESCRIPTION

IMAGE PROCESSING DEVICE

TECHNICAL FIELD

[0001] The present invention relates to an image processing device in which compression/expansion of image data can be carried out.

BACKGROUND ART

[0002] In recent years, in addition to displaying image data, electronic apparatuses such as mobile telephones also display and store image data that has been captured by electronic camera capabilities equipped therein. Consequently such electronic apparatuses require complex processing to be performed on large amounts of image data and in general these use image processing devices in which a CPU is used (for example, see patent documents 1 and 2). FIG. 3 shows one example of a conventional image processing device. An image processing device 101 has a bus architecture in which a high-speed bus 10 and a peripheral bus 12 are linked via a bus bridge 11, and various functional circuits are connected to both the buses 10 and 12. That is to say, the high-speed bus 10 is connected to a CPU 13 for carrying out computation and control necessary for image processing and the like, a ROM 14 that stores a processing program of the CPU 13, and a RAM 15 used as a work

area and the like for the computation carried out by the CPU 13. The peripheral bus 12 is connected to a frame memory 16 that stores image expansion data from an electronic camera 2 or image expansion data to which image compression data from a host device 4 is expanded and displays this data on a display panel 3 such as an LCD, a compression/expansion circuit 17 for carrying out compression of image expansion data and expansion of image compression data, a transceiving FIFO (first in first out) memory 18 for carrying out transceiving of image compression data from and to the host device 4, and a general-purpose timer circuit 19 and the like. The image processing device 101 includes a frame memory register 20 in which data of the frame memory 16 is read and written by the CPU 13, a compression/expansion circuit register 21 in which data of the compression/expansion circuit 17 is read and written by the CPU 13, and a data transceiving register 22 in which data of the data transceiving FIFO memory 18 is read and written by the CPU 13. It should be noted that in the present application, image compression data refers to image data that is compressed and image expansion data refers to image data that has not been compressed.

[0003] Image expansion data from the electronic camera 2 is stored in the frame memory 16 and displayed on the display panel 3 and is also read in by the CPU 13 via the frame memory register 20 and the peripheral bus 12 and compressed using the

compression/expansion circuit 17 and the RAM 15 and the like. The resulting image compression data is written into the data transceiving FIFO memory 18 via the peripheral bus 12 and the data transceiving register 22 and sent in order to the host device 4. On the other hand, image compression data from the host device 4 is received at the data transceiving FIFO memory 18 and read in order into to the CPU 13 via the data transceiving register 22 and the peripheral bus 12, then expanded using the compression/expansion circuit 17 and the RAM 15 and the like. The resulting image expansion data is stored in the frame memory 16 via the peripheral bus 12 and the frame memory register 20 and displayed on the display panel 3.

[0004] Patent Document 1: Japanese Patent Application Laid-open No. 2001-350461

Patent Document 2: Japanese Patent Application Laid-open No. 2002-77709

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0005] Image processing is performed in this manner, but to continue achieving processes for higher picture quality of the images displayed and for variety of performances of moving and still pictures, even greater speed is required in image processing. To achieve greater speed in image processing it is common to

increase the speed of all the functional circuits including the CPU, but when giving consideration to such factors as power consumption and cost, it is also essential in addition to this to make the CPU operate efficiently.

[0006] The present invention was conceived for the above reasons and it is an object thereof to provide an image processing device capable of enabling a CPU to operate more efficiently and thus achieve greater speed in image processing.

MEANS FOR SOLVING THE PROBLEM

[0007] In order to solving the aforementioned problems, an image processing device according to a preferred embodiment of the present invention is an image processing device in which a high-speed bus and a peripheral bus are linked via a bus bridge and in which connected to the high-speed bus and the peripheral bus are a CPU for carrying out computation and control of image processing, a data transceiving FIFO memory for carrying out transceiving of image compression data with a host device, a frame memory for storing image expansion data and displaying this data on a display panel, and a compression/expansion circuit for carrying out compression of image expansion data and expansion of image compression data, wherein the CPU and the frame memory are connected to the high-speed bus and the data transceiving FIFO memory is connected to the peripheral bus.

[0008] In this image processing device, it is preferable that the compression/expansion circuit is connected to the high-speed bus.

[0009] An image processing device according to another preferred embodiment of the present invention is an image processing device which has an CPU-direct instruction bus, a CPU-direct data bus, and a high-speed bus, and in which connected to these buses are a CPU for carrying out computation and control of image processing, a ROM for storing a processing program of the CPU, a RAM used as a work area for the computation carried out by the CPU, a data transceiving FIFO memory for carrying out transceiving of image compression data with a host device, a frame memory for storing image expansion data and displaying this data on a display panel, and a compression/expansion circuit for carrying out compression of image expansion data and expansion of image compression data, wherein the CPU and the ROM are connected to the CPU-direct instruction bus, the CPU, the RAM, and the frame memory are connected to the CPU-direct data bus, and the CPU and the data transceiving FIFO memory are connected to the high-speed bus.

[0010] In this image processing device, it is preferable that the compression/expansion circuit is connected to the CPU-direct data bus.

EFFECTS OF THE INVENTION

[0011] According to the present invention, in the image processing device, the frame memory, which has a large volume of data, is connected to a bus having relatively high processing capability, and the data transceiving FIFO memory, which has a comparatively small volume of data, is connected to a bus having relatively low processing capability, and therefore the CPU can be made to operate efficiently and thus achieve greater speed in image processing overall.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] [Fig. 1] FIG. 1 is a block diagram of an image processing device according to a preferred embodiment of the present invention.

[Fig. 2] FIG. 2 is a block diagram of an image processing device according to another preferred embodiment of the present invention.

[Fig. 3] FIG. 3 is a block diagram of a conventional image processing device.

EXPLANATION OF REFERENCE NUMERALS

[0013] 1, 5 image processing device

2 electronic camera

3 display panel

4 host device

10 high-speed bus

12 peripheral bus

13, 23 CPU

16 frame memory

17 compression/expansion circuit

18 data transceiving FIFO memory

20 frame memory register

21 compression/expansion circuit register

22 data transceiving register

24 CPU-direct instruction bus

25 CPU-direct data bus

BEST MODE FOR CARRYING OUT THE INVENTION

[0014] Hereinafter, preferred embodiments of the present invention are described with reference to the drawings. FIG. 1 is a block diagram of an image processing device according to a preferred embodiment of the present invention. An image processing device 1 has a bus architecture in which a high-speed bus 10, which operates at a high frequency of 75 MHz for example, and a peripheral bus 12, which operates at a frequency of 25 MHz for example, are linked via a bus bridge 11, and various functional circuits are connected to both the buses 10 and 12. That is, the high-speed bus 10 is connected to a CPU 13 for carrying out

computation and control necessary for image processing and the like, a ROM 14 that stores a processing program of the CPU 13, and a RAM 15 used as a work area and the like for the computation carried out by the CPU 13, and furthermore is connected to a frame memory 16 that stores image expansion data from the electronic camera 2 or image expansion data to which image compression data from the host device 4 is expanded and displays this data on the display panel 3 such as an LCD, and a compression/expansion circuit 17 for carrying out compression of image expansion data and expansion of image compression data. The peripheral bus 12 is connected to a transceiving FIFO memory 18 for carrying out transceiving of image compression data from and to the host device 4, and a general-purpose timer circuit 19 and the like. The image processing device 1 includes a frame memory register 20 in which data of the frame memory 16 is read and written by the CPU 13, a compression/expansion circuit register 21 in which data of the compression/expansion circuit 17 is read and written by the CPU 13, and a data transceiving register 22 in which data of the data transceiving FIFO memory 18 is read and written by the CPU 13. It should be noted that the compression/expansion circuit 17 specifically includes circuits such as a JPEG circuit used in the compression/expansion of still pictures or an MPEG circuit used in the compression/expansion of moving pictures. Furthermore, when the image processing device 1 is used in an electronic

apparatus such as a mobile telephone, the host device 4 includes a processor device that controls main unit functions of that apparatus.

[0015] Image expansion data from the electronic camera 2 is stored in the frame memory 16 and displayed on the display panel 3 and is also read in by the CPU 13 via the frame memory register 20 and the high-speed bus 10 and compressed using the compression/expansion circuit 17 and the RAM 15 and the like. The resulting image compression data is written into the transceiving FIFO memory 18 via the peripheral bus 12 and the data transceiving register 22 and sent in order to the host device 4. On the other hand, image compression data from the host device 4 is received at the data transceiving FIFO memory 18 and read in order into to the CPU 13 via the data transceiving register 22 and the peripheral bus 12, then expanded using the compression/expansion circuit 17 and the RAM 15 and the like. The resulting image expansion data is stored in the frame memory 16 via the high-speed bus 10 and the frame memory register 20 and displayed on the display panel 3.

[0016] Here, since the high-speed bus 10 operates at a high frequency of 75 MHz for example, the image expansion data is read in from the frame memory 16 to the CPU 13 at high speed and written from the CPU 13 to the frame memory 16 at high speed. Since the frame memory 16 is connected to the same bus as the RAM 15 used

as a work area for computation, overhead time, which is wasted time due to bus switching, can be eliminated in series of computations. Thus, the CPU operates efficiently in the transfer of image expansion data having large volumes of data and therefore the speed of the overall image processing is increased. Furthermore, data transfers between the CPU 13 and the compression/expansion circuit 17 are via the high-speed bus 10 and therefore the speed of the overall image processing is further increased. On the other hand, the peripheral bus 12 operates on a frequency of 25 MHz for example, and therefore the writing in of image compression data to the data transceiving FIFO memory 18 and the reading out to the CPU 13 are conducted at a comparatively slow speed. However, the image compression data is for example from one-tenth to one-hundredth of the image expansion data and a comparatively small amount of data, and therefore the speed of the overall image processing does not drop very much.

[0017] In this way, according to the image processing device 1, the frame memory 16, which has a large volume of data, is connected to the high-speed bus 10 having relatively high processing capability, and the data transceiving FIFO memory 18, which has a comparatively small volume of data, is connected to the peripheral bus 12 having relatively low processing capability, and therefore the CPU 13 can be made to operate efficiently and thus achieve greater speed in image processing overall. It should

be noted that the data transceiving FIFO memory 18 is connected to the peripheral bus 12 because if there are too many functional circuits connected to the high-speed bus 10, the load capacity of the high-speed bus 10 increases and the operable frequency is reduced by that amount.

[0018] In the image processing device 1, the compression/expansion circuit 17 is connected to the high-speed bus 10, but in case the compression/expansion circuit 17 to be used undergoes comparatively little reading and writing by the CPU 13, it may be connected to the peripheral bus 12.

[0019] Next, another preferred embodiment of an image processing device according to the present invention is described with reference to FIG. 2. An image processing device 5 has a bus architecture provided with a CPU-direct instruction bus 24 that directly links the CPU 23 and the ROM 14, a CPU-direct data bus 25 that directly links the CPU 23 and the RAM 15, and the aforementioned high-speed bus 10. For example, a TCM (tightly coupled memory) instruction bus in an ARM based processor system, a TCM data bus, and an AMBA (advanced microcontroller bus architecture) bus respectively correspond to the CPU-direct instruction bus 24, the CPU-direct data bus 25, and the high-speed bus 10. It should be noted that this can also be configured so as to be provided with the peripheral bus 12 (not shown in the drawing) as required.

[0020] The CPU-direct data bus 25 is further connected to the aforementioned frame memory 16 and the compression/expansion circuit 17. The high-speed bus 10 is connected to the aforementioned data transceiving FIFO memory 18 and timer circuit 19 and the like. The image processing device 5, as with the image processing device 1, includes the frame memory register 20, the compression/expansion circuit register 21, and the data transceiving register 22.

[0021] The CPU-direct instruction bus 24 and the CPU-direct data bus 25 carry out reading and writing operations at for example one cycle of the basic operational clock of the CPU 23. On the other hand, the high-speed bus 10 carries out reading and writing operations at for example 5 to 10 cycles. Consequently, compared to the image processing device 1, in the image processing device 5, the image expansion data is read in from the frame memory 16 to the CPU 23 at an even greater speed and writes from the CPU 23 to the frame memory 16 at an even greater speed.

[0022] In this way, according to the image processing device 5, the frame memory 16, which has a large volume of data, is connected to the CPU-direct data bus 25 having relatively high processing capability, and the data transceiving FIFO memory 18, which has a comparatively small volume of data, is connected to the high-speed bus 10 having relatively low processing capability, and therefore even greater speed can be achieved in image

processing overall. It should be noted that the data transceiving FIFO memory 18 is connected to the high-speed bus 10 because the load capacity of the high-speed bus 10 does not increase very much since the frame memory 16 is shifted to the CPU-direct data bus 25.

[0023] In the image processing device 5, the compression/expansion circuit 17 is connected to the CPU-direct data bus 25, but in case the compression/expansion circuit 17 to be used undergoes comparatively little reading and writing by the CPU 23, it may be connected to the high-speed bus 10.

[0024] Herein description has been given concerning image processing devices according to embodiments of the present invention, but the present invention is not limited to these embodiments and various design modifications are possible within the scope of the claims. For example, when there is no electronic camera 2 in the electronic apparatus in which the image processing device 1 or 5 is to be used, it is possible to omit a function for storing image expansion data from the electronic camera 2 to the frame memory 16. And of course it is possible whenever required to not include the general-purpose timer circuit 19 and to include other necessary functional circuits.